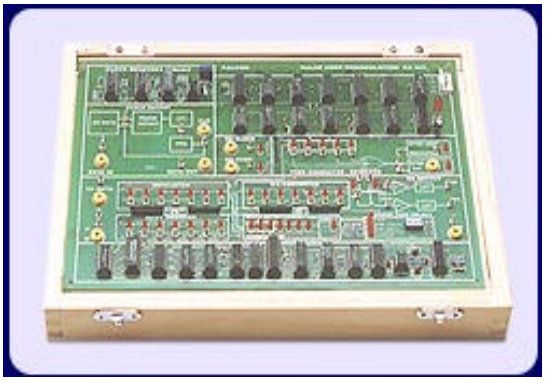
TLD-04: PULSE CODE DEMODULATION RECEIVER



This module has been designed to allow the students to see the decoding of original encoded signal sent through PCM transmitter kit. The receiver kit "phase locks" to the input pulse stream to derive the clock information.
Moreover, by the use of pseudo-random binary sequence, the synchronization between transmitter and receiver is established.

Features :

- 2 channel Time Division Demultiplexed PCM receiver.
- Real-time operation using fast mode or examination of data and control signals decoding on LED's.
- Low pass filters allow original signals to be reconstructed.
- Single bit error detection, when odd or even parity is slected in the transmitter.
- Single bit error detection, when odd or even parity is selected in the transmiter.
- Various test points provided on-board.

Technical Specifications :

- Input channels **:** 2 numbers TDM pulse code modulated data.
- Receiver clock **:** Generated by phase-lock loop
- Parity check facility **:** Even, Odd, Hamming
- Low pass filter **:** 3.4 KHz (cut-off)
- Power Supply **:** +5V, +/-12V

List of Experiments :

- Study of 2 - channel Time Division Demultiplexing and pulse code demodulation.
- Study of Error Check Code Logic using Odd parity, Even parity and Hamming parity.
- Study of effect of single bit error detection in Odd parity and Even parity mode and single bit error correction in Hamming Parity mode.
- To learn the function of phase lock loop (PLL) to a receiver clock generator and frequency syntheziser.